REMARKS

This Amendment is in response to the Office Action mailed December 27, 2007. Claims 1, 4, 7-14, 17-26, 29, 30, 34-36, 39-48, 52, and 53 were pending. In this response, claims 12, 21, 30, 36, 34, 45, and 48 have been amended. No claims have been added or cancelled. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 103

The Examiner rejects claims 1, 4, 7-10, 12-14, 17-19, 21, 23-26, 29, 30, 34, 36, 48, 52 and 53 under 35 U.S.C. § 103(a) as being unpatentable over Rice, et al. (U.S. Patent No. 6,816,961) in view of Goodman & Miller, "A Programmer's View of Computer Architecture." Applicants respectfully disagree.

Rice describes a system that swaps bytes by selecting which field in a destination register receives which field from a source register (Rice, column 2, lines 45-51). Specifically, Rice describes a source register that includes a plurality of operation fields (Rice, column 2, lines 1-10). The fields contain two parts, a 3-bit portion and 5-bit codes that trigger the various operations (*See* Rice, column 8, Table II). Rice explicitly teaches that "five bits [are] devoted to the operation field" where a 5-bit sequence determines what operation is to be performed (Rice, column 7, lines 51-53).

Goodman describes instruction formats (Goodman, page 199). Goodman describes, at only a very high level, that a two address format for an instruction specifies that an address may act as both an addend and the address for storing a result (Goodman, page 199).

Claim 1 recites in part:

> responsive to receiving a single packed shuffle instruction designating, with 3 bits, a first register storing a first operand having a set of L data elements and designating, with 3 bits, a second register storing a second operand having a set of L control elements, wherein the first operand and second operand are of a same size and each of the L data elements and L control elements are of a same size, and wherein each one of the L control elements is divided into three portions, the first portion being a flush to zero bit occupying the most significant bit of each control element wherein the flush to zero bit alone controls whether a resultant element is flushed to zero, the second portion being a position selection field that is at least $\log_2 L$ bits wide and indicates a position of one of said L data elements, and a third portion reserved for another purpose,
> (Emphasis Added)

The Applicants respectfully submit that Rice and Goodman, alone or in combination, fail to describe each and every feature as claimed in claim 1.

Rice describes a processing architecture that includes field swapping capability. As taught by Rice:

> [A] second source register 508 includes a number of condition fields 700. Three bits of the condition field 700 is devoted to the result field select value and five bits is devoted to the operation field. The result field select bits select which source field 512 is stored in a result field 528. The operation fields are coupled to their respective operand processors 704.
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> (Emphasis Added) (Rice, column 7, lines 50-56)

Thus, Rice teaches that an operand specifies an address of a selected data value and an operation to be performed on that value. Furthermore, Rice explicitly states that three bits are devoted to addressing, while five bits are devoted to specifying a function to be performed. Because Rice operates on bytes of data, the addressing and function specification portions are required to occupy the entire byte of an operand. Thus, all 8 bits of each source field in Rice are taught as being devoted to only one of two purposes.

The Applicants, however, claim that responsive to a single instruction, which includes a first portion being a flush to zero portion, a second portion being a position selection portion, and

a third portion that is reserved for another purpose. Thus, the instruction enables a flush to zero capability and position selection, while also enabling another purpose. As such, the instruction and control element claimed by the Applicants is simply not taught or suggested by Rice, because Rice devotes two fields of an operand to only two purposes (*See* Rice, column 7, lines 50-56).

The Examiner states:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the ability to perform operations on result fields other than the operations indicated by operation fields "00000" and "00001" (i.e., no modification and clearing) since it has been held that eliminating an element and its function is not sufficient to patentably distinguish over the prior art (See In re Karlson CCPA 1963).
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> (Final Office Action, mailed 12/27/07, page 3)

Applicants respectfully submit, however, that Applicants' claimed control elements is divided into three portions with a first portion being a flush to zero portion, a second portion being a position selection field, and a third portion for another purpose. Thus, not only does the control element provide for position selection and flush to zero, but other purposes are enabled by the third portion of the claimed control element. As indicted in the MPEP, "the omission of an element and retention of its function is an indicia of unobviousness" (See *In re Edge*, 359 F.2d 896, 149 USPQ 556 (CCPA 1966)). Thus, where applicants claim a control element with three portions each for a different purpose, the required two element structure and function described in Rice is omitted. Furthermore, the flush to zero function is retained while also enabling additional functions reserved to the third field of the control element.

Since many features claimed by the applicants are not explicitly described by Rice (See Final Office Action, mailed 12/27/07, pages 2-3), and the control element claimed by the

Applicants omits elements required by Rice, while both retaining the flush to zero functionality and further enabling additional functions via a third portion of the control element, Rice must fail to describe or suggest the features claimed by the Applicants.

Furthermore, Goodman merely discusses address formatting, without reference to processor instructions, control elements, or control element configurations, Goodman also must fail to teach or suggest the instruction and control element claimed by the Applicants.

Therefore, the Applicants respectfully submit that Goodman and Rice, alone or in combination, fail to describe or suggest each and every element of claim 1. Thus, claim 1 is not rendered obvious by Rice in view of Goodman, for at least the reasons noted above. Furthermore, claims 4, 7-10, 12-14, 17-19, 21, 23-26, 29, 30, 34, 36, 48, 52 and 53 contain similar features and limitations to those discussed above with respect to claim 1. Thus, for similar reasons, claims 4, 7-10, 12-14, 17-19, 21, 23-26, 29, 30, 34, 36, 48, 52 and 53 are also not rendered obvious by Rice in view of Goodman, for similar reasons to those advanced with respect to claim 1. Therefore, the Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 4, 7-10, 12-14, 17-19, 21, 23-26, 29, 30, 34, 36, 48, 52 and 53 under 35 U.S.C. § 103(a) as being unpatentable over Rice in view of Goodman.

The Examiner rejects claims 11, 20, 22 and 35 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman and, further in view of the Examiner's taking of Official Notice. The Official notice, however, fails to teach or suggest the shortcomings of Rice and Goodman discussed above. Thus, Applicants respectfully requests that the Examiner withdraw the rejection of claims 11, 20, 22 and 35 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman and, further in view of the Official Notice.

The Examiner rejects claims 39-43, 45 and 47 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman and, further in view of Hoyle, et al. (U.S. Patent Application Publication No. 2005/0188182). Similar to the discussion above, with respect to independent claim 1, Rice and Goodman, alone or in combination, similarly fails to describe or suggest each and every element of amended independent claims 39 and 45. Hoyle discusses a system where instructions perform byte intermingling from two source operands and store a result in a third result operand (Hoyle, Abstract). Because the various three-operand byte intermingling instructions merely perform predefined intermingling operations (*See* Hoyle, Table 9), Hoyle similarly fails to teach or suggest the limitations noted above. Therefore, for reasons similar to those discussed with respect to claim 1, Rice, Goodman, and Hoyle, alone or in combination fail to describe or suggest the limitations recited in claims 39 and 45, along with their respective dependent claims. The Applicants therefore respectfully requests that the Examiner withdraw the rejection of claims 39-43, 45 and 47 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman and, further in view of Hoyle.

The Examiner rejects claims 44 and 47 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman, in view of Hoyle, and further in view of the Examiner's taking of Official Notice. The Official notice, however, fails to teach or suggest the shortcomings of Rice, Goodman, and Hoyle, as discussed above. Therefore, Applicants respectfully requests that the Examiner withdraw the rejection of claims 44 and 47 under 35 U.S.C. § 103(a) as being unpatentable over Rice, in view of Goodman, in view of Hoyle, and further in view of the Official Notice.

Conclusion

Applicant reserves all rights with respect to the applicability of the doctrine of equivalents. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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By_____

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